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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/054,964	01/25/2002	Nobuya Sumiyoshi	KY-172	8804

7590 11/24/2006

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EXAMINER	
TORRES, JUAN A	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 11/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

A

Office Action Summary	Application No.	Applicant(s)	
	10/054,964	SUMIYOSHI, NOBUYA	
	Examiner	Art Unit	
	Juan A. Torres	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2002*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☒ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-9,11 and 12* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

Figures 4 and 5 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated (see specification pages 1-7). See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities:

a) The recitation in page 4 line 8 "oscillator)as shown" is improper because it is not properly constructed; it is suggested to be changed to "oscillator) as shown"

b) The recitation in page 11 lines 15-20 "In FIG. 1, which is a circuit construction of a data transmission system according to a first embodiment of the present invention, the data transmission system has a transmitting side (computer side) including a transmitting circuit 9 and a receiving side (liquid crystal device." is improper because it

is not properly constructed; it is suggested to be changed to "In FIG. 1, which is a circuit construction of a data transmission system according to a first embodiment of the present invention, the data transmission system has a transmitting side (computer side) including a transmitting circuit 9 and a receiving side (liquid crystal device)." (emphasis added).

c) The recitation in page 18 line 2 "VS" is improper (see figures 1 and 3 and page 17 line 13); it is suggested to be changed to "V_S"

Appropriate correction is required.

Claim Objections

Claim 10 is objected to because of the following informalities: the recitation in line 14 of claim 10 "sad" is improper because it lacks of antecedent basic; it is suggested to be changed to "said". Appropriate correction is required.

Allowable Subject Matter

Claims 1-9 and 11-12 are allowable.

Claim 10 is allowable is the above objections are overcome.

The following is an examiner's statement of reasons for allowance: claims 1-12 are allowed because the references cited fail to teach, as applicant has, a sampling clock generator circuit comprising a ring oscillator including series-connected m first inverters connected to a first power supply line, where m is an odd number equal to or larger than 3, a delay line including series-connected 2 m or 2 m-1 second inverters connected to a second power supply line, for delaying an externally supplied clock signal, and a PLL circuit including a voltage controlled oscillation circuit for controlling

an oscillation frequency of said ring oscillator by controlling a voltage of said first power supply line, a voltage of said second power supply line being set substantially equal to the voltage of said first power supply line and the delayed clock obtained by said second inverters is used as a sampling clock; a sampling clock generator circuit comprising a ring oscillator including series-connected m first inverters connected to a first power supply line, where m is an odd number equal to or larger than 3, a delay line including series-connected 2 m or 2 m-1 second inverters connected to a second power supply line, for delaying an externally supplied clock, a first PLL circuit including a voltage controlled oscillation circuit for controlling an oscillation frequency of said ring oscillator by controlling a voltage of said first power supply line, a second PLL circuit for generating a control voltage for locking the clocks outputted said inverters of said delay line by comparing the phase of the external clock with the phase of the clocks outputted from said delay line, and a voltage setting circuit for setting the voltage of said second power supply line on the basis of the voltage of said first power supply line and the control voltage, the delayed clock obtained from said second inverters is used as a sampling clock; a data receiving device comprising a ring oscillator including series-connected m first inverters connected to a first power supply line, where m is an odd number equal to or larger than 3, a delay line including series-connected 2 m or 2 m-1 second inverters connected to a second power supply line, for delaying an externally supplied clock and outputting the thus delayed external clock from said second inverters, a PLL circuit including a voltage controlled oscillation circuit for controlling an oscillation frequency of said ring oscillator by controlling a voltage of said first power

supply line, and a serial/parallel converter circuit for converting the transmitted serial data into a parallel data in units of n data, sad serial/parallel converter circuit being supplied with the delayed clock obtained from said second inverters by setting the voltage of said second power supply line substantially equal to the voltage of said first power supply line; and a data receiving device comprising a ring oscillator including series-connected m first inverters connected to a first power supply line, where m is an odd number equal to or larger than 3; a delay line including series-connected 2 m or 2 m-1 second inverters connected to a second power supply line, for delaying an externally supplied clock and outputting the thus delayed external clock from said second inverters; a first PLL circuit including a voltage controlled oscillation circuit for controlling an oscillation frequency of said ring oscillator by controlling a voltage of said first power supply line; a second PLL circuit for comparing a phase of the external clock with a phase of the clock outputted from said inverters of said delay line and generating a control voltage for locking the clock outputted from said inverters of said delay line; a voltage setting circuit for setting the voltage of said second power supply line on the basis of the voltage of said first power supply line and the control voltage; and a serial/parallel converter circuit for converting the transmitted serial data into a parallel data in units of n data, said serial/parallel converter circuit being supplied with the delayed clock obtained from said second inverters, as the applicant has claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Chi (US 5239274 A) discloses a voltage-controlled ring oscillator using complementary differential buffers for generating multiple phase signals. Mizuno (US 6683503 B2) discloses an oscillation circuit, and a semiconductor integrated circuit device which includes a clock distribution system of low jitter and low skew employing the oscillation circuit. Chi and Mizuno don't disclose a delay line including series-connected 2 m or 2 m-1 second inverters connected to a second power supply line, for delaying an externally supplied clock signal, and a PLL circuit including a voltage controlled oscillation circuit for controlling an oscillation frequency of said ring oscillator by controlling a voltage of said first power supply line, a voltage of said second power supply line being set substantially equal to the voltage of said first power supply line and the delayed clock obtained by said second inverters is used as a sampling clock.

This application is in condition for allowance except for the following formal matters:

See above.

Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Juan Alberto Torres
11-13-2006